Interoperability with AD9152 DAC

Document revision record

<table>
<thead>
<tr>
<th>Rev.:</th>
<th>Date:</th>
<th>Initiator:</th>
<th>Changes:</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>161010</td>
<td>TGN</td>
<td>Initial Release</td>
</tr>
<tr>
<td>1.2</td>
<td>161101</td>
<td>JCA</td>
<td>One configuration added LMF=421</td>
</tr>
<tr>
<td>1.3</td>
<td>170313</td>
<td>JCA</td>
<td>Three configurations added LMF=124, LMF=222 and LMF=422. Deterministic latency test cases added.</td>
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<td>1.4</td>
<td>171114</td>
<td>TGN</td>
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</tr>
<tr>
<td>1.5</td>
<td>171128</td>
<td>TGN</td>
<td>Final review comments included</td>
</tr>
</tbody>
</table>
1 Introduction
The Comcores JESD204B IP core is a high-speed point-to-point serial interface intellectual property (IP). The JESD204B IP core has been hardware-tested with a number of selected JESD204B-compliant ADC (analog-to-digital converter) and DAC (digital-to-analog) devices.

The purpose of this document is to provide the reader with detailed understanding of how the Inter-Operability Testing (IOT) between Comcores JESD204B IP core and Analog Devices AD9152 DAC has been carried out.

Comcores's JESD204B IP implementation is a fully silicon agnostic implementation of the standard [1] and comes as fully separate RX and TX link entities with the option of including a transport layer function.

For this interoperability the JESD204B IP has been implemented at a Xilinx ZC706 evaluation board in order to carry out the test of the TX function.

2 Scope
This document is intended for a technical audience (engineering, marketing, customer support) with an understanding on serial interface protocols and converter technology. Engineering background on digital design is required.

The scope of this document is to present the hardware test bed setup and components, the test methodology and test cases as well as the test results. The scope is to provide integration engineers with sufficient knowledge to adapt and verify the cores in a customized environment and application.

3 Applicable and Reference Documents

<table>
<thead>
<tr>
<th>Document ID</th>
<th>Title</th>
</tr>
</thead>
</table>
| [1]         | JESD204B.01  
Serial Interface for Data Converters (Revision of JESD204B, July 2011). Date January 2012 |

4 Acronyms and Definitions
A/D = Analog to Digital  
ASIC = Application Specific Integrated Circuit  
ASSP = Application Specific Standard Product  
CF = Control bits per frame  
CS = Control Bits per sample  
D/A = Digital to Analog  
F = Number of Octets
5 Xilinx Zynq-7000 – ADI AD9152 Hardware IOT Setup

A Xilinx Zynq-7000 Development Kit is used with the ADI AD9152 daughter card module installed on the development board’s FMC connector. A schematic of the setup is shown in Figure 1.

- The AD9152 EVM derives power from the Zynq-7000 FMC connector.
- A DAC device reference clock is generated at the DAC EVM.
- Both the FPGA and DAC device clock must be sourced from the same clock source.

![Figure 1 - System setup for interoperability test](image-url)
5.1 Test bed components

The hardware test bed consists of the following items:

1. Xilinx Zynq-7000 All Programmable SoC ZC706 Evaluation Kit (Zynq evaluation card)  
3. USB cable x1, Power adapter x1

To make the given setup work some modifications need to be added to the AD9152-FMC-EBZ in order to make the given setup work properly. The DAC must be configured and controlled via the FMC connector which implies some small changes in the hardware of the AD9152 EVM. These changes are described in Figure 2 and Figure 3.

![Figure 2](image1.png)

Figure 2 - Set the PIC microcontroller in reset state to take over the control of the SPI.

![Figure 3](image2.png)

Figure 3 - Force level converter to be enabled.
The hardware setup is shown in Figure 4 - Photo of the hardware setup with the ZC706 and AD9152 EVM.

![Image of hardware setup with ZC706 and AD9152 EVM]

**Figure 4 - Photo of the hardware setup with the ZC706 and AD9152 EVM**

### 5.2 Hardware Test Bed Clocking

The clock is generated on the LMK device (TI - LMK04828 - Ultra Low Jitter Synthesizer and Jitter Cleaner) on the DAC evaluation board and provided to the Zynq evaluation card via FMC as shown in figure 1. The Comcores JESD204B IP Cores utilize a 40 bit serdes interface which compares to AD9152 interfaces which also uses a 40 bit serdes interface.

### 5.3 Hardware Test Bed FPGA Pin Out

<table>
<thead>
<tr>
<th>Node Name</th>
<th>Direction</th>
<th>Location</th>
<th>I/O Standard</th>
</tr>
</thead>
<tbody>
<tr>
<td>gt0_gtxtxp_o</td>
<td>OUTPUT</td>
<td>AF2</td>
<td>LVDS</td>
</tr>
<tr>
<td>gt0_gtxtn_o</td>
<td>OUTPUT</td>
<td>AF1</td>
<td>LVDS</td>
</tr>
<tr>
<td>gt1_gtxtxp_o</td>
<td>OUTPUT</td>
<td>AE4</td>
<td>LVDS</td>
</tr>
<tr>
<td>gt1_gtxtn_o</td>
<td>OUTPUT</td>
<td>AE3</td>
<td>LVDS</td>
</tr>
<tr>
<td>gt2_gtxtxp_o</td>
<td>OUTPUT</td>
<td>AH2</td>
<td>LVDS</td>
</tr>
<tr>
<td>gt2_gtxtn_o</td>
<td>OUTPUT</td>
<td>AH1</td>
<td>LVDS</td>
</tr>
</tbody>
</table>
A system view of the test setup is shown in figure 1. The system-level diagram shows how different modules connect in this design. In this setup an external reference clock of 400MHz is sourced to the AD9152 EVM through the SMA. The EVM buffers the reference clock and provides the same device clock to the FPGA and AD9152.

### 5.4 AD9152 Hardware Test Bed HDL Setup

The test bed consist of a top level entity “jesd204b_ad9152” which instantiates the test and configuration logic, the serdes and the jesd204b core “csc_jesd204b_tx”, and also routes the two blocks together and to the Input and Output interfaces (clocks, FMC, LEDs and pushbuttons).

The JESD204B TX core does not include serdes module but provide a multiple of 10bit wide interface to them. The width of this interface is controlled with a generic NO_SERDES_WORDS. In this test bed a 160 bit interface is used for the serdes. The IP core also include a CPU interface to which the test and configuration logic is connected allowing reading and writing of the internal register values during the CORE operation.

### 5.5 AD9152 Hardware Test Bed Software

The test and configuration software is running in a Xilinx Vivado tcl shell. It has access to the CPU interface of the JESD204B RX core, the SPI interface of the AD9152, the SPI interface of the AD9516 (Clock Generator), as well as the test bed core module. It is able to reconfigure on the fly the various operating parameters. This allows the software to control the test parameters, device configurations, and run times. It is also able to read out the test results from the data validator as well as the error indicators.
The test and configuration software provides a console based interface allowing the user to initialize and monitor the automated test sequence as well as the IP core and serdes status. It provides direct access to the IP core and test bed registers. This allows full control of the IP core.

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>test_ALL</td>
<td>Run all IOT tests. Syntax: <strong>test_ALL</strong></td>
</tr>
<tr>
<td>test_CGS1</td>
<td>Transmitter data link layer IOT test. For detailed test description see Table 4. Syntax: <strong>test_CGS1</strong></td>
</tr>
<tr>
<td>test_TL1</td>
<td>Transmitter transport layer IOT test. For detailed test description see Table 5. Syntax: <strong>test_TL1</strong></td>
</tr>
<tr>
<td>test_TL2</td>
<td>Transmitter transport layer IOT test. For detailed test description see Table 5. Syntax: <strong>test_TL2</strong></td>
</tr>
<tr>
<td>jesd_wr</td>
<td>Write to the JESD204B core registers. Syntax: <strong>jesd_wr</strong> [address - 32bit hex] [data - 32bit hex] Example: <strong>jesd_wr</strong> 00000004 04030201</td>
</tr>
<tr>
<td>jesd_rd</td>
<td>Read from the JESD204B core registers. Syntax: <strong>jesd_rd</strong> [address - 32bit hex] Example: <strong>jesd_rd</strong> 00000004</td>
</tr>
<tr>
<td>spi_dac_clkgen_wr</td>
<td>Write to the AD9516 registers. Syntax: <strong>spi_dac_clkgen_wr</strong> [address - 16bit hex] [data - 8bit hex] Example: <strong>spi_dac_clkgen_wr</strong> 0004 01</td>
</tr>
<tr>
<td>spi_dac_clkgen_rd</td>
<td>Read from the AD9516 registers. Syntax: <strong>spi_dac_clkgen_rd</strong> [address - 16bit hex] Example: <strong>spi_dac_clkgen_rd</strong> 0004</td>
</tr>
<tr>
<td>spi_dac_wr</td>
<td>Write to the AD9152 registers. Syntax: <strong>spi_dac_wr</strong> [address - 16bit hex] [data - 8bit hex] Example: <strong>spi_dac_wr</strong> 0004 01</td>
</tr>
<tr>
<td>spi_dac_rd</td>
<td>Read from the AD9152 registers. Syntax: <strong>spi_dac_rd</strong> [address - 16bit hex] Example: <strong>spi_dac_rd</strong> 0004</td>
</tr>
</tbody>
</table>

Table 2 - Relevant software commands for the AD9152 IOT test bed

5.6 Device Configuration Overview

The JESD204B IP core parameters (L, M and F) in this hardware checkout are natively supported by the AD9152 device's configuration registers. The transceiver data rate, sampling clock frequency, and other JESD204B parameters comply with the AD9152 operating conditions.

The hardware checkout testing implements the JESD204B IP core with the following parameter configuration.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Test Mode #1</th>
<th>Test Mode #2</th>
<th>Test Mode #3</th>
<th>Test Mode #4</th>
<th>Test Mode #5</th>
<th>Test Mode #6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line rate (Gbps)</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>LMF</td>
<td>112</td>
<td>124</td>
<td>211</td>
<td>222</td>
<td>422</td>
<td>421</td>
</tr>
<tr>
<td>HD</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>S</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>N</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
</tbody>
</table>
6 Test description and results

6.1 Hardware Checkout Methodology

The following section describes the test objectives, procedure, and the passing criteria.

The following test cases have been conducted as part of the IOT:

- Transmitter data link layer (6.2)
- Transmitter transport layer (6.3)
- Deterministic latency (6.4)

6.2 Transmitter Data Link Layer

This test area covers the test cases for Code Group synchronization (CGS), Frame Synchronization and Initial Lane Synchronization (CGS1). On link startup, the receiver issues a synchronization request and the transmitter transmits /K28.5/ characters. After code group synchronization, the receiver assumes that the first non-/K28.5/ symbol marks the start of a frame. If the transmitter emits an initial lane alignment sequence, the first non-/K28.5/ symbol will always be /K28.0/. The receiver assumes that a new frame starts every 8 octets. The initial lane synchronization is carried out before the start of user payload data. At a well-defined point in time, all the transmitters issue a dedicated lane alignment character /A/= /K28.3/. This character is used to align the individual lanes.

6.2.1 CGS test cases

The CGS test case is described in Table 4 - CGS test cases.

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>CGS1</td>
<td>Check the Code Group Synchronization, Frame Synchronization and Initial Lane Synchronization</td>
<td>1. Force sync_b for JESD TX asserted high to force the TX to only transmit /K25.5/ symbols. 2. Release sync_b for the JESD RX to take over. After CGS the TX is transmitting the Initial Lane Alignment Sequence.</td>
<td>• Code Group Synchronization achieved for all lanes  • Frame Synchronization achieved for all lanes  • ILAS checksum ok  • Initial Lane Synchronization for all lanes</td>
</tr>
</tbody>
</table>

Table 4 - CGS test cases
6.3 Transmitter Transport Layer
To verify the data integrity of the payload data stream through the TX JESD204B IP core and transport layer, the DAC JESD204B IP core is configured to check short transport layer test pattern that is transmitted from FPGA test pattern generator. The DAC JESD204B IP core checks the short transport layer test patterns based on \( F = 1 \) configuration. The short test pattern has a duration of one frame period and is repeated continuously for the duration of the test.

To verify the stability of JESD link the FPGA is configured to generate a PRBS test pattern. The test is a success if no errors detected, i.e. none of the following errors observed at the DAC:

- Bad running disparity
- Not in table
- Unexpected control character

6.3.1 TL test cases
The TL test cases are described in Table 5 - Transmitter Transport Layer Test cases.

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
</table>
| TL1       | Check the transport layer mapping using short transport layer test pattern as specified in the parameter configuration. | • Set each octet to a unique value at the FPGA  
• JESD204B sample interface.  
• Set the expected corresponding values in the DAC.  
• Run the test.  
• Check if there is a match for all values. | • The DAC register bit SHORT_TPL_TEST_3.SHORT_TPL_FAIL is not asserted. |
| TL2       | Verify the data transfer from digital to digital domain. | • Generate a PRBS input at the JESD TX sample interface and receive these correctly at DAC. | No of the following error detected at the JESD RX node:  
• Bad running disparity  
• Not in table  
• Unexpected control character |

Table 5 - Transmitter Transport Layer Test cases

6.4 Deterministic Latency (Subclass 1)
Figure below shows a block diagram of the deterministic latency test setup. The AD9516-1 clock generator on the AD9144 EVM provides periodic SYSREF pulses for both the DAC and JESD204B IP core. The period of SYSREF pulses is configured to two Local Multi Frame Clocks (LMFC). The SYSREF pulse restarts the LMF counter and realigns it to the LMFC boundary.
The FPGA generates a 16-bit digital sample with a value of 8000 hexadecimal number at the transport layer. The most significant bit of this digital sample has a logic 1 and this bit is an output pin at the FPGA. This bit is probed at channel 1 of the oscilloscope. The DAC analog channel is probed at channel 2 of the oscilloscope. With two's complement value of 8000h, a pulse with the amplitude of negative full range is expected at channel 1 of the DAC analog. The time difference between the pulses at channel 1 (t0) and channel 2 (t1) is measured. This is the total latency of the JESD204B link, the DAC digital blocks, and the analog channel.

**Test Case**

<table>
<thead>
<tr>
<th>Test Case</th>
<th>Objective</th>
<th>Description</th>
<th>Passing Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>DL1</td>
<td>Measure the total latency.</td>
<td>Measure the time difference between the rising edge of the pulses at oscilloscope channel 1 and 2.</td>
<td>The latency should be consistent.</td>
</tr>
<tr>
<td>DL2</td>
<td>Re-measure the total latency after DAC power cycle and FPGA reconfiguration.</td>
<td>Measure the time difference between the rising edge of pulses at oscilloscope channel 1 and 2.</td>
<td>The latency should be consistent.</td>
</tr>
</tbody>
</table>

**6.5 Test Results**

For each test case stating a compliance statement according the following terms are provided:

<table>
<thead>
<tr>
<th>Result</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pass</td>
<td>The Device Under Test (DUT) was observed to exhibit conformant behavior</td>
</tr>
<tr>
<td>Pass with comments</td>
<td>The DUT was observed to exhibit conformant behavior. However, an additional explanation of the situation is included, such as due to time limitations only a portion of the testing was performed.</td>
</tr>
</tbody>
</table>
The DUT was observed to exhibit non-conformant behavior

The DUT was observed to exhibit behavior that is not recommended.

From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.

The following table shows the results for test cases CGS1, TL1 and TL2 with different values of L, M, F, K, subclass, data rate, sampling clock, link clock, and SYSREF frequencies.

<table>
<thead>
<tr>
<th>Test #</th>
<th>L</th>
<th>M</th>
<th>F</th>
<th>K</th>
<th>Sub-class</th>
<th>Lane rate (Gbps)</th>
<th>Sampling Clock (MHz)</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>16</td>
<td>1</td>
<td>8</td>
<td>400</td>
<td>PASS</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>16</td>
<td>1</td>
<td>8</td>
<td>200</td>
<td>PASS</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>32</td>
<td>1</td>
<td>8</td>
<td>800</td>
<td>PASS</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>16</td>
<td>1</td>
<td>8</td>
<td>400</td>
<td>PASS</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>16</td>
<td>1</td>
<td>8</td>
<td>800</td>
<td>PASS</td>
</tr>
<tr>
<td>6</td>
<td>4</td>
<td>2</td>
<td>1</td>
<td>32</td>
<td>1</td>
<td>4</td>
<td>400</td>
<td>PASS - A console results printout can be found in Figure 7 and Figure 8</td>
</tr>
</tbody>
</table>

Table 6 - Test Results for Interoperability testing

In Figure 7 - Console printout for test CGS1 and Figure 8 - Console printout for test TL2 the result of test case #1 is shown to be successful. All tests are PASSING.

Figure 7 - Console printout for test CGS1
In Table 7 - Deterministic Latency Test Results the results of the deterministic latency tests are shown.

<table>
<thead>
<tr>
<th>Test #</th>
<th>L</th>
<th>M</th>
<th>F</th>
<th>K</th>
<th>Subclass</th>
<th>Lane rate (Gbps)</th>
<th>Sampling Clock (MHz)</th>
<th>Allowed Deviation (ns)</th>
<th>Total Latency Result (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>16</td>
<td>1</td>
<td>8</td>
<td>200</td>
<td>PASS (4.7)</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>4</td>
<td>16</td>
<td>1</td>
<td>8</td>
<td>200</td>
<td>PASS (4.6)</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>32</td>
<td>1</td>
<td>8</td>
<td>200</td>
<td>PASS (4.5)</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>16</td>
<td>1</td>
<td>8</td>
<td>400</td>
<td>PASS (4.6)</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>16</td>
<td>1</td>
<td>8</td>
<td>800</td>
<td>PASS (5.0)</td>
</tr>
<tr>
<td>6</td>
<td>4</td>
<td>2</td>
<td>1</td>
<td>32</td>
<td>4</td>
<td>1</td>
<td>4</td>
<td>400</td>
<td>PASS (8.6)</td>
</tr>
</tbody>
</table>

Table 7 - Deterministic Latency Test Results

All tests are PASSING.

An example of the measurement is given in Figure 9. The measurement is performed from the rising edge of Ch. 3 to the falling edge of Ch. 4. As described previously and shown in Figure 5 a negative signal is expect on
the output. With two's complement value of 8000h, a pulse with the amplitude of negative full range is expected at channel 1 of the DAC analog. This is also the case for this measurement.

The oscilloscope resolution are set to 80 ns and as seen in the figure a delay of 368.3 ns is measured in Figure 9 between the rising and falling edge of the two signals. Performing several sweeps and making an average of the latency variation gives the results shown in Table 7.

![Figure 9 - Deterministic Latency Measurement for LMF=422 Configuration](image)

### 7 How to perform the IOT test

#### 7.1 Quick IOT setup guide

Comcores is offering a software setup for conducting the test cases. For inquiry about the software environment to conduct these tests please send mail to info@comcores.com

This chapter describes the necessary steps required to reproduce the test results.

1. Change directory to `JESD204B_IOT\AD9152`
2. Double-click at shortcut “Start IOT”. This opens a TCL Shell, program the FPGA, configure the system and run the IOT tests.
3. Each test reports are listed as either “******** Test: [testcase], PASSED ********” or “******** Test: [testcase], FAILED ********”

7.2 Link Delay setup without known delays

It is observed that if the LMFC Var and LMFC Del registers at the DAC side are not correctly configured, then it leads to random PRBS test failures. Hence, these registers are fine-tuned by reading registers DYN_LINK_LATENCY_x (DAC register 0x302). By repeatedly power-cycling and taking this measurement, the minimum and maximum delays across power cycles can be determined and used to calculate LMFC Var and LMFC Del. For information on how to calculate these register values, refer D9152 datasheet. Setting LMFC Del appropriately ensures that all the corresponding data samples arrive in the same LMFC period. Then, LMFC Var is written into the receive buffer delay (RBD) to absorb all link delay variation. This ensures that all data samples have arrived before reading. By setting these to fixed values across runs and devices, deterministic latency is achieved. The following table gives the calculated LMFC Var and LMFC Del for each mode. The same values are also programmed in the scripts corresponding to each mode.

To get the DYN_LINK_LATENCY values perform the following steps multiple times:

1. Change directory to ..\JESD204B_IOT\AD9152
2. Power cycle hardware, i.e. FPGA board.
3. Double-click at shortcut “Start DYN_LINK_LATENCY measure”. This opens a TCL Shell and start the DYN_LINK_LATENCY measurement.
4. Select the JESD configuration, to be tested.
5. The FPGA is now programmed, and the clock and JESD are configured. When the script ends, the value of the DYN_LINK_REGISTER is printed “DYN_LINK_LATENCY: XX”.
6. Remember this value for the later calculation of the “LMFC Var” and “LMFC Del” parameters.
7. Close the TCL Shell terminal and restart. These steps should be performed minimum ten times.

When enough values are obtained (minimum 10), calculate the two parameters from this instructions:
To implement this new parameters in the existing IOT test flow, open the following file:

```
.JESD204B_IOT\AD9152\ad9152_IOT.tcl
```

Change the values for a given configuration, e.g. updating the values for configuration LMF=422, then change the values for the following variables:

```
set LMFC_DELAY_LMF422_8G 0a
set LMFC_VAR_LMF422_8G 03
```

Next time the IOT test is performed, the updated values are used.

7.3 LMFC Var and LMFC Del values used for the IOT test

```
set LMFC_DELAY_LMF124_8G 0a
set LMFC_VAR_LMF124_8G 03
set LMFC_DELAY_LMF222_8G 08
set LMFC_VAR_LMF222_8G 04
set LMFC_DELAY_LMF422_8G 0a
set LMFC_VAR_LMF422_8G 03
set LMFC_DELAY_LMF421_4G 0c
set LMFC_VAR_LMF421_4G 03
```
8 Conclusion

An interoperability test between Comcores JESD204B IP and Analog Devices AD9152 DAC has been carried out successfully. The test has been carried out by implementing Comcores JESD204B IP on a Xilinx evaluation board that connects to the AD9152 DAC Evaluation board.

The transmitter data link layer and transport link layers have been successfully tested in various configuration and deterministic has been verified.

In each test case, the TX JESD204B IP core successfully initializes from CGS phase, ILA phase, and until user data phase. Data integrity is checked at the DAC data path layer using the PRBS-15 pattern. The data path PRBS verifies that the AD9152 data path receives and correctly decodes the data. The data path PRBS also verify these processes:

- JESD204B parameters of the transmitter and receiver are matched
- Lanes of the receiver are mapped appropriately
- Lanes have been appropriately inverted, if necessary
- The start-up routine has been implemented correctly

In deterministic latency test, there is consistent total latency across the JESD204B link and DAC analog channels. For the latency to be deterministic, it is important that the SYSREF gets sampled at the same time at both the DAC and FPGA, and each SYSREF needs to be phase aligned at the same LMFC boundary.

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