COMCORES

JESD204C ADI Interoperability Test

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Contents

1 Introduction

The Comcores JESD204C IP core is a high-speed point-to-point serial interface intellectual property (IP). An interoperability test has been carried out between Comcores JESD204C IP core and Analog Devices JESD204C IP. The interoperability test has been performed by simulating Comcores TX with ADI RX and Comcores RX with ADI TX. The setup has been tested with selected configurations as agreed with ADI.

The purpose of this document is to provide the reader with detailed understanding of how the Inter-Operability Testing (IOT) between Comcores JESD204C IP core and Analog Devices JESD204C IP has been carried out. The document includes architecture of the respective IPs, list of configurations tested, as well as the simulation results in the form of waveforms.

2 Interoperability Planning

2.1 Tasks

To carry out the interoperability the following steps were planned:

- Running ADI testbench (sanity check)
- Comcores testbench with ADI Tx
- Comcores testbench with ADI Rx
- ADI testbench with Comcores Tx
- ADI testbench with Comcores Rx
- Interoperability Report

2.1.1 Running ADI testbench (sanity check)

The ADI_JESD204C_IP includes the Transmitter/Receiver IP instantiated with the testbench top level in the module tb_top. In order to perform the sanity check on the ADI IP, it needs to simulate with the provided test cases. After verifying successful simulation, the sanity check is concluded to be complete. The simulation of ADI_JESD204C_IP is running with VCS (vcs/2017.12-SP2 version).

2.1.2 Comcores testbench with ADI TX

To check the interoperability of ADI TX IP with Comcores IP, the ADI TX IP was instantiated in Comcores testbench. The Interoperability can be checked by connecting ADI TX to Comcores RX. Testing ADI TX IP in Comcores environment with Comcores testcases can verify the interoperability of the IPs. Figure 1 Indicates the block diagram of test setup 1 for testing the compatibility of Comcores Rx with ADI Tx.

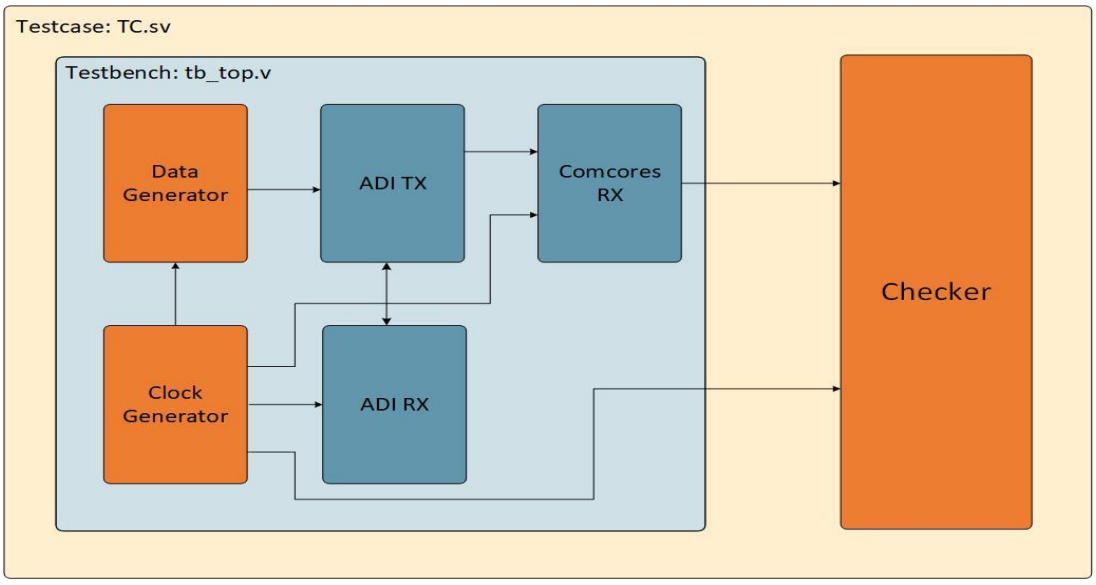

Figure 1: Interoperability test setup 1 (ADI TX and Comcores RX)

2.1.3 Comcores testbench with ADI RX

Similarly, to check the interoperability of ADI RX IP with Comcores IP, the ADI RX IP was instantiated in Comcores testbench. The Interoperability can be checked by connecting ADI RX to Comcores TX as shown in figure 2.

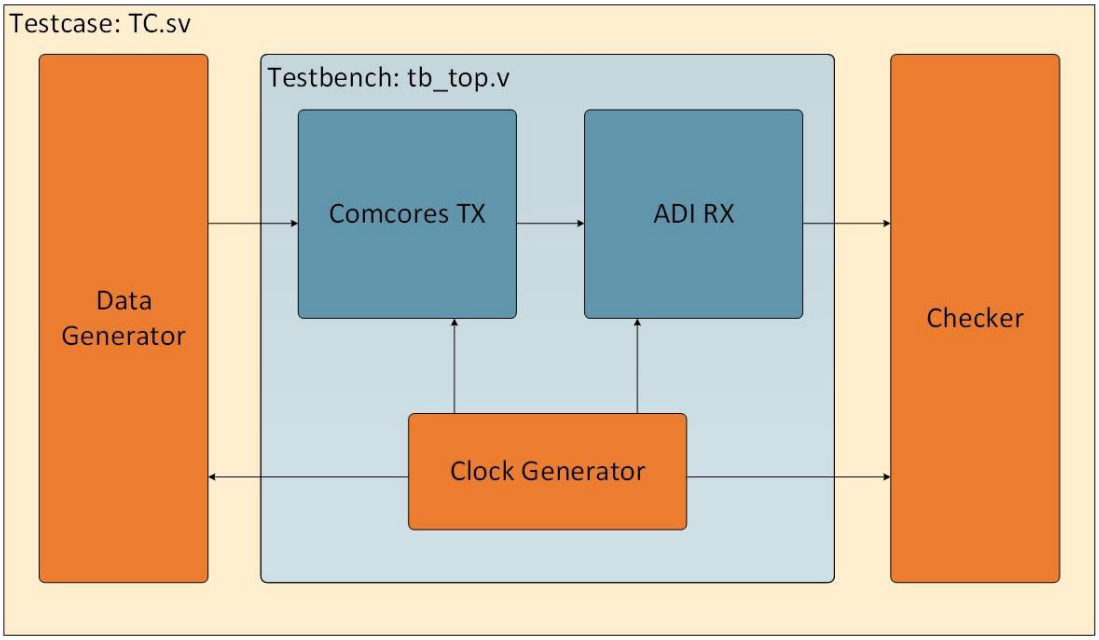

Figure 2: Interoperability test setup 2 (Comcores TX and ADI RX)

2.1.4 ADI testbench with Comcores TX

To check the interoperability of ADI TX IP with Comcores IP the ADI TX IP has been instantiated in ADI testbench. The Interoperability can be checked by connecting ADI RX to Comcores TX.

2.1.5 ADI testbench with Comcores RX

To check the interoperability of ADI RX IP with Comcores IP, the ADI RX IP was instantiated in ADI testbench. The Interoperability can be checked by connecting ADI TX to Comcores RX.

2.1.6 Interoperability Report

The Interoperability report includes all the steps taken to check the Interoperability in detail and the results obtained by that.

3 Architecture

The system architecture of the Comcores JESD204C IP and ADI JESD204C IP test bench are shown in figure 3 and figure 4 respectively. JESD204C is the interface standard developed by JEDEC for high-speed serial data communication. It is used for connecting the ADCs and DACs to the design providing the line speed of up to 32 Gbps per lane. It also ensures the alignment and synchronization of data signal.

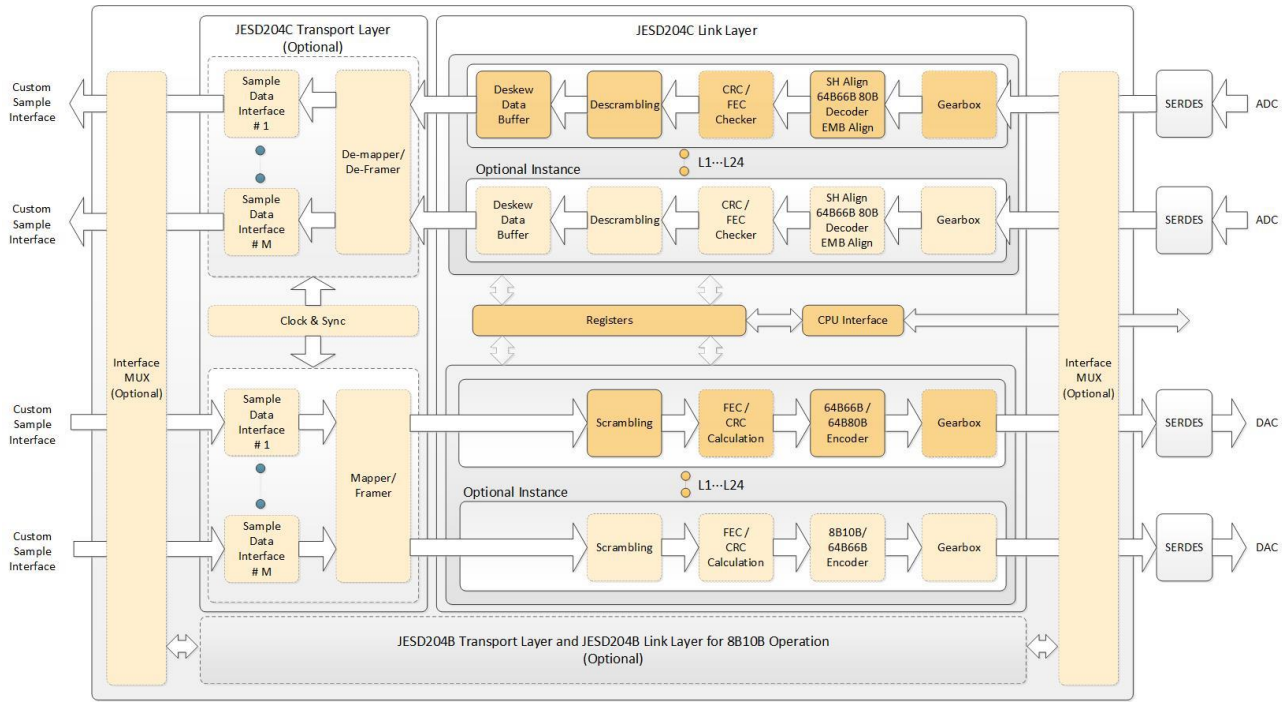

Figure 3: Comcores JESD204C Architecture

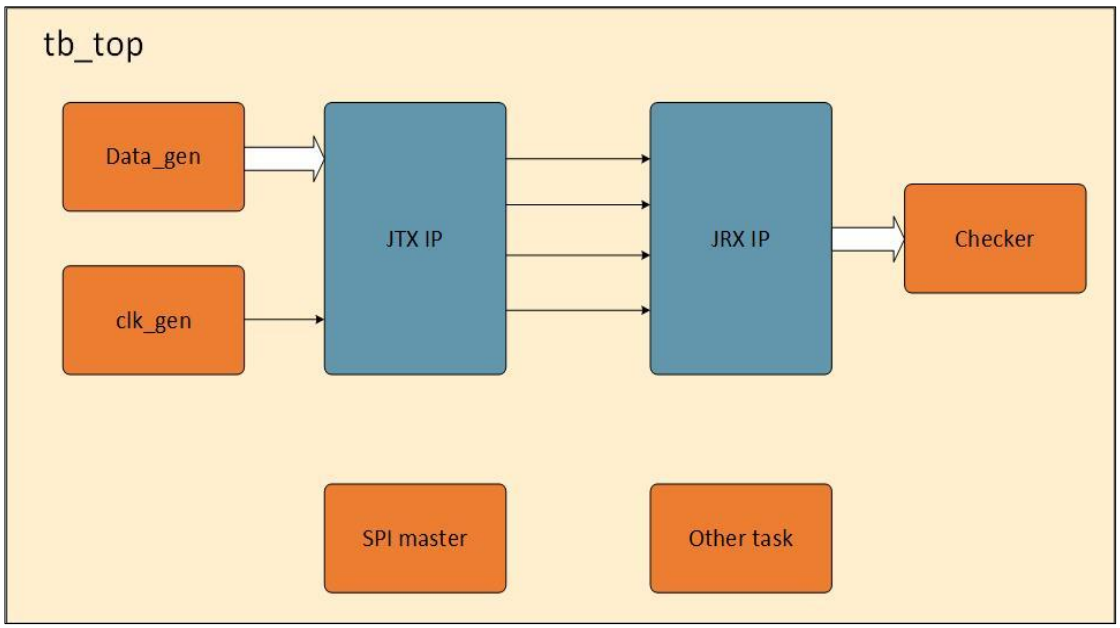

Figure 4: Analog Devices JESD204C Testbench Architecture

4 Testing Setup

The main strategy for testing the interoperability between ADI and Comcores IP was to test the ADI TX vs Comcores RX and vice versa. Both setups were organized in the same testbench “tb_top.v” isolated by the ifdef condition. The “ADI_2_COM” defines the setup where ADI TX is connected to the Comcores RX and “COM_2_ADI” defines the setup where Comcores TX is instantiated with the ADI RX. (illustrated in Figure 5 and Figure 6). Changing mode from “COM_2_ADI” and “ADI_2_COM” can be done by commenting out the unwanted define mode at top of the testbench “tb_top.v”. The testbench “tb_top.v” is instantiated with the testcase “TC.sv” which is driven by the Make file. Furthermore, to test all the configurations at once, there is a script “vcs_tests_run.sh” containing all the valid configurations which will continuously run all the configurations and generate different log file for each test configuration. Please note, while changing the setup from ADI_2_COM to COM_2_ADI or vice versa, the clock driving the checker should be the same as receiver sample clock. Similarly, the sample clock for transmitter and the clock driving data generator should be the same.

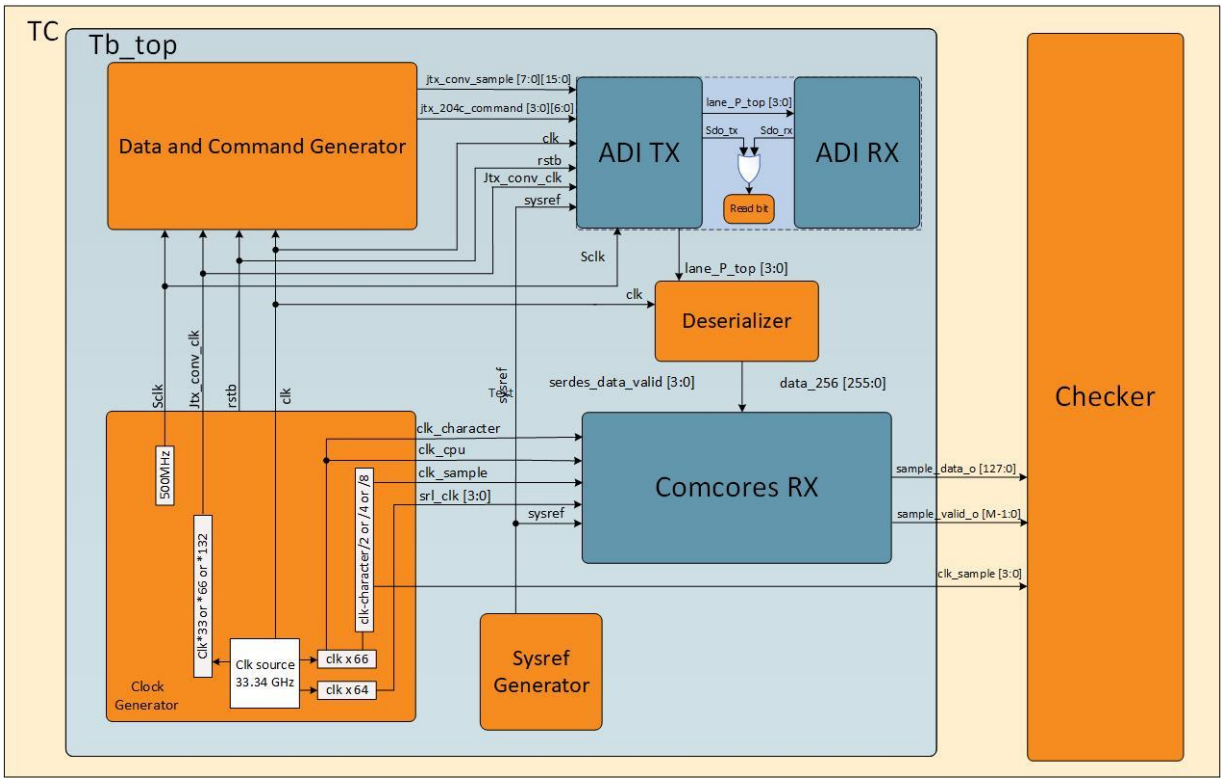

Figure 5: Interoperability test setup 1 (ADI TX and Comcores RX)

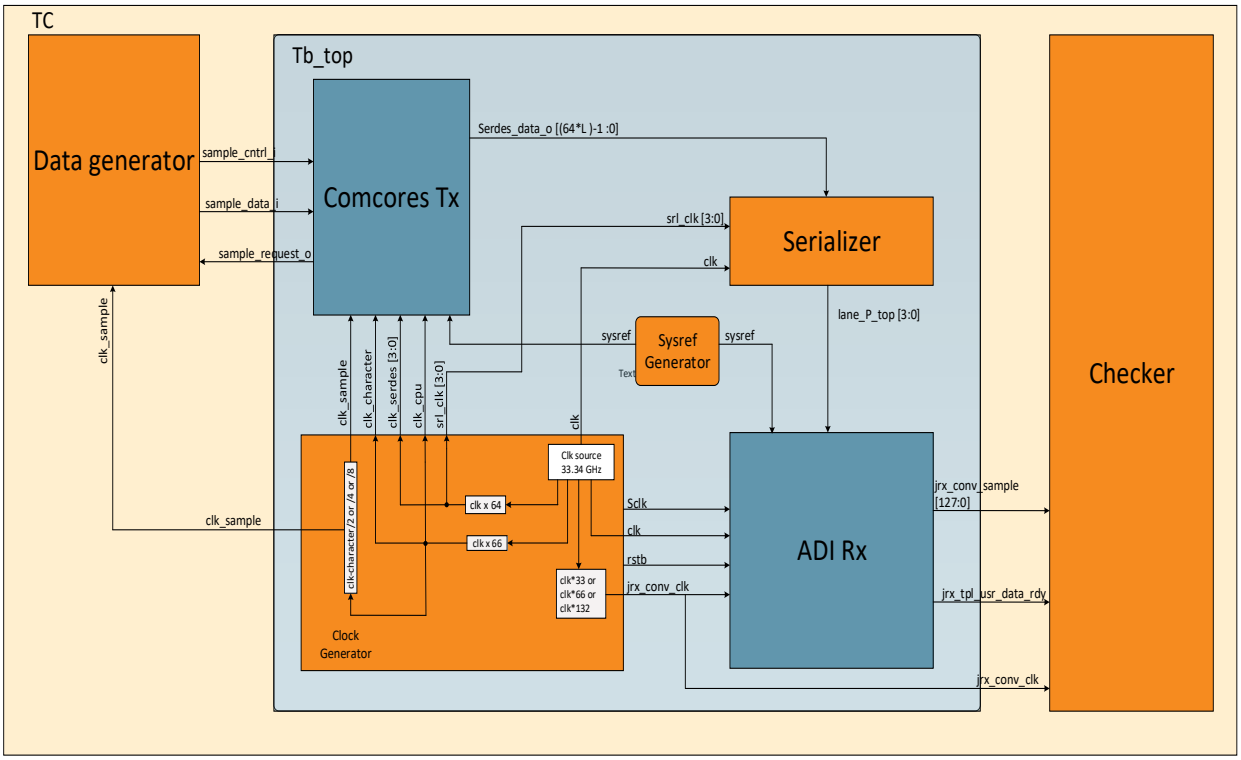

Figure 6: Interoperability test setup 2 (Comcores TX and ADI RX)

The clock allocation for the test setup is as outlined in Table 1.

Table 1: Clock allocation

Setup	Data generator	Transmitter	Receiver	Checker
ADI_2_COM	ADI data generator driven by jtx_conv_clk	jtx_conv_clk	clk_sample	Comcores data checker driven by clk_sample
COM_2_ADI	Comcores data generator driven by clk_sample	clk_sample	jtx_conv_clk	Comcores data checker driven by jtx_conv_clk

5 Configurations

For the interoperability test the configurations shown in table 2 have been targeted.

Table 2. Configurations interoperability tested for ADI and Comcores JESD204C IP

Parameters	Config 1	Config 2	Config 3	Config 4	Config 5	Config 6	Config 7
N	16	16	16	16	16	16	16
L	2	4	1	1	1	2	1
M	8	8	8	2	2	2	2
S	1	1	1	1	2	2	4
F	8	4	16	4	8	4	16
K	32	64	16	64	32	64	16

The configurations have been run for Subclass =1, serdes data width = 64, JESD number of sample interface = S

5.1 Interface

Interfaces supported for CPU configurations are as follow:

- Comcores: AXI, APB, AVALON, I2C,
- ADI: SPI

For Interoperability test setup AXI and SPI interfaces are used for configuring Comcores and ADI IP respectively. The CPU clock for both interfaces is 500 MHz which is independent of any other clock in the setup.

6 Clocking Relations

The clock relationships shown in table 3 have been used for the interoperability test. Timescale 1ns/1ps

Table 3. Configuration supported by the ADI and Comcores JESD204C IP.

Clock Name	Clock Relation (Relationship in periods of clocks)
clk	0.030 ns (33.34 GHz)
ser_clk	clk
srl_clk	clk*64
clk_serdes	clk*64
clk_character	clk*66
jtx_conv_clk	If F=4 then clk*33 (ser_clk*33) If F=8 then clk*66 (ser_clk*66) If F=16 then clk*132 (ser_clk*132)
jrx_conv_clk	jtx_conv_clk
clk_sample	If CR=0 then clk*66 (clk_character) If CR=1 then clk*33 (clk_character/2) If CR=2 then clk*16.5 (clk_character/4) If CR=3 then clk*8.25 (clk_character/8)

*CR= Clock Ratio; F= No of Frames.

Figure 7 represents the clock relations between different clocks with respect to the source clock “clk”. The period of source clock “clk” is 0.030 ns, and the figure represents periods for different clocks with respect to the period of clock “clk”, where “ser_clk” is equal to “clk”. “srl_clk” and “clk_serdes” are serdes clock maintaining the 64/66 ratio with device clock “clk_character”. “jtx_conv_clk” and “jrx_conv_clk” are sample clock for ADI IP, which are selected based on JESD number of frames and “clk_sample” is the sample clock for Comcores IP, which is selected based on clock ratio defined in Comcores design.

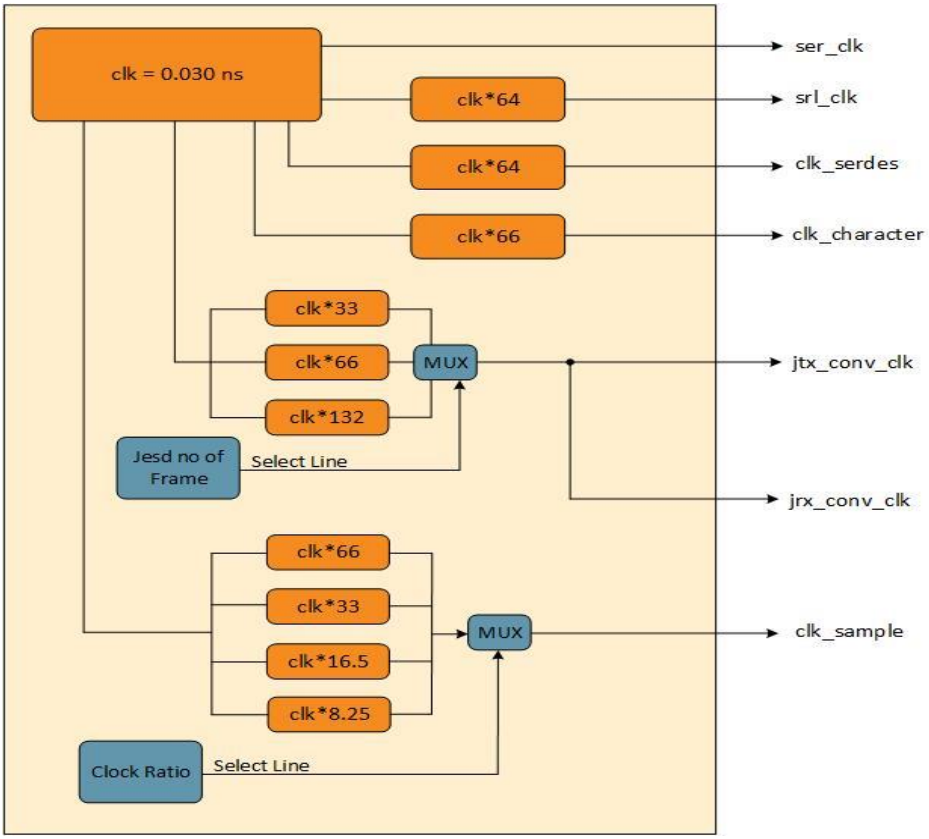

Figure 7: Interoperability test setup clock relations

7 Results

The configurations were successfully executed demonstrating seamless compliance between Comcores JESD204C IP and ADI JESD204C implementation. The results for the testing are shown in Table 4.

Table 4. Result for all the Configurations

Parameters	Config 1	Config 2	Config 3	Config 4	Config 5	Config 6	Config 7
N	16	16	16	16	16	16	16
L	2	4	1	1	1	2	1
M	8	8	8	2	2	2	2
S	1	1	1	1	2	2	4
F	8	4	16	4	8	4	16
K	32	64	16	64	32	64	16
ADI_2_COM	Passing	Passing	Passing	Passing	Passing	Passing	Passing
COM_2_ADI	Passing	Passing	Passing	Passing	Passing	Passing	Passing

The setup in which ADI Transmitter is connected to Comcores Receiver is successfully simulated using VCS (vcs/2017.12-SP2 version). Figure 8 indicates the sent and received samples by the IPs for the configuration N=16, L=2, M=8, S=1, F=8, K32 which are successfully compared and verified by the checker implemented in the setup.

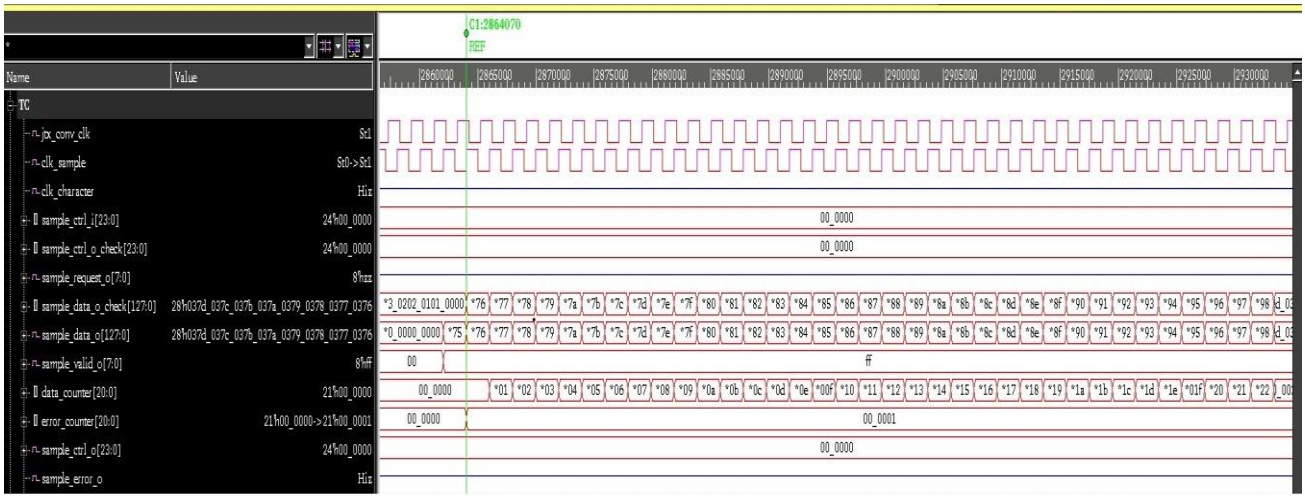

Figure 8: output waveform for configuration N16L2M8S1F8K32 in ADI_2_COM setup.

Figure 9 indicates the successful transmission of data from Comcores Transmitter to ADI receiver for the configuration of N=16, L=2, M=8, S=1, F=8, K32.

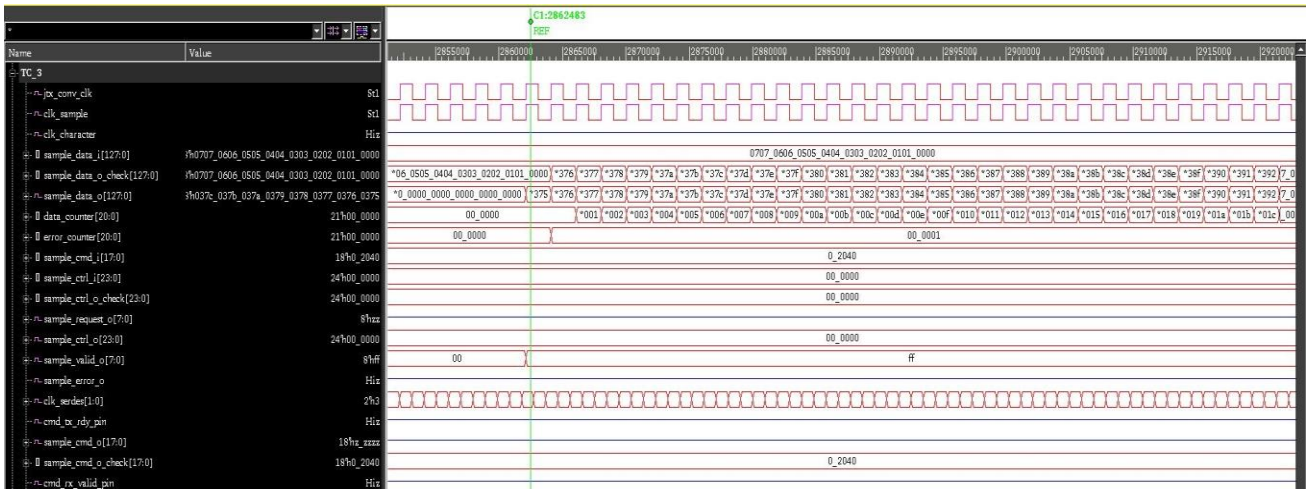

Figure 9: output waveform for configuration N16L2M8S1F8K32 in COM_2_ADI setup.

8 Conclusion

The interoperability test for Comcores and ADI JESD204C IP is concluded successfully with the passing result of all the seven testcases as agreed with ADI. As ADI IP is sending and receiving serialized data, the serializer and deserializer block has been implemented in the setup. The IPs are tested with the CRC3 and CRC12 enabled in the Comcores JESD204C IP. The successful implementation of ADI TX with Comcores RX and vice versa represents the compatibility capability of both the IPs. The setup is now ready to test the compatibility of both IPs with other test configurations if needed in the future.